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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): En-Hsing Chen, et al.

Title: NAND MEMORY ARRAY INCORPORATING MULTIPLE SERIES  
SELECTION DEVICES AND METHOD FOR OPERATION OF SAME

Application No.: 10/729,865

Filed:

December 5, 2003

Examiner: Nguyen, Van Thu T.

Group Art Unit:

2824

Atty. Docket No.: 023-0029

Confirmation No.:

8494

March 15, 2005

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**INFORMATION DISCLOSURE STATEMENT**  
**37 C.F.R. § 1.97(b)**

Dear Sir:

Pursuant to 37 C.F.R. § 1.56, § 1.97 and § 1.98, the undersigned brings to the Examiner's attention in the above-identified application the patents, publications, applications or other information identified in the attached:

- ☒ Form(s) PTO/SB/08A (5 page(s), with copy of 4 reference(s)).
- ☒ Form(s) PTO/SB/08B (2 page(s), with copy of 20 reference(s)).
- ☒ Listing of Pending Applications (1 page(s), with copy of no application(s)).
- ☐ Other: N/A

Citation of such information shall not be construed as (i) an admission that the information necessarily is, or corresponds to, prior art with respect to the instant invention, (ii) a representation that a search has been made, other than as described herein, or (iii) an admission that the information cited herein is, or is considered to be, material to patentability as defined in § 1.56(b).

For each item of information listed that is not in the English language, the undersigned has provided a concise explanation of the relevance through (i) an English language abstract, (ii) an English language equivalent application, or (iii) if cited in a search report or other action by a foreign patent office in a counterpart foreign application, an English language version of the search report or action that indicates the degree of relevance found by the foreign office.

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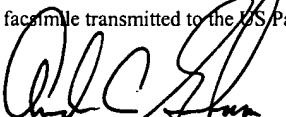
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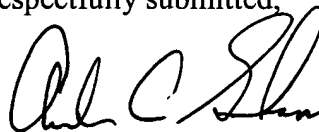
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- ☐ This Information Disclosure Statement is filed within three months of the filing date of a national application other than a continued prosecution application under § 1.53(d) or within three months of entry of the national stage as set forth in § 1.491 in an international application. Therefore, no fee is required.
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Andrew C. Graham	Date

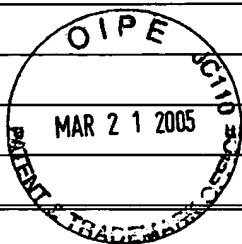
Respectfully submitted,



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EXPRESS MAIL LABEL: _____
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PTO/SB/08A (Substitute for form 1449/PTO)	Attorney Docket No.: 023-0029
	Application No.: 10/729,865
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	First Named Inventor: En-Hsing Chen et al.
	Filing Date: December 5, 2003
	Group Art Unit: 2824
	Examiner Name: Van Thu Nguyen
Sheet 1 of 5	Date Submitted: March 15, 2005



U.S. PATENT DOCUMENTS						
Examiner Initials*	Cite No. <sup>1</sup>	Document Number Number-Kind Code <sup>2</sup> (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	
	AA	4,142,176	02-27-1979	Dozier		
	AB	4,543,594	09-24-1985	Mohsen et al.		
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	AN	JA 62-142363	06-25-1987			
	AO	JA 62-155568	07-10-1987			
	AP	JA-2001-358237	12-26-2001			
	AQ	JA-2002-280467	09-27-2002			
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<sup>1</sup>Applicant's unique citation designation number (optional).

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<sup>4</sup>For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document.

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PTO/SB/08A (Substitute for form 1449/PTO)	Attorney Docket No.: 023-0029
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<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>	First Named Inventor: En-Hsing Chen et al.
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	AR	5,715,194	02-03-1998	Hu	
	AS	5,751,012	05-12-1998	Wolstenholme et al.	
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	BD	6,185,122 B1	02-06-2001	Johnson et al.	

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	BI	6,188,611 B1	02-13-2001	Endoh et al.	
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	BZ	6,515,888	02-04-2003	Johnson et al.	
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	CO					
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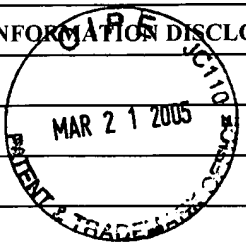
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	CQ	US-2002/0021587 A1.	02-21-2002	Sakui et al	
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	DA	US-5,812,457	09-1998	Arase	
	DB				
	DC				

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#### NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. <sup>1</sup>	Include name of author (in CAPITAL LETTERS), title of article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
	AA	DURISETY, CHANDRA SEKHAR ACHARYULU, "Analysis and Characterization of Single-Poly Floating Gate Devices in 0.35um PDSOI Process", A Thesis Presented for the Master of Science Degree, The University of Tennessee, Knoxville, December 2002, pp. i-viii and 1-80.	
	AB	EVANS, ROBERT J., ET AL., "Energy Consumption Modeling and Optimization for SRAM's," IEEE Journal of Solid-State Circuits, Vol. 30, No. 5, May 1995, pp. 571-579.	
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	AE	KIM, KYU-HYOUN, ET AL., "An 8-Bit-Resolution, 360-μs Write Time Nonvolatile Analog Memory Based on Differentially Balanced Constant-Tunneling-Current Scheme (DBCS)," IEEE Journal of Solid-State Circuits, Vol. 33, No. 11, November 1998, pp. 1758-1762.	
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	AH	KITANO, YOSHITAKA, ET AL., "A 4-Mbit Full-Wafer ROM," IEEE Journal of Solid-State Circuits, Vol. SC-15, No. 4, August 1980, pp. 686-693.	
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	AJ	LIN, HORNG-CHIH, ET AL., "Ambipolar Schottky-Barrier TFTs," IEEE Transactions on Electron Devices, Vol. 49, No. 2, February 2002, pp. 264-270.	
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	AL	NISHIHARA, TOSHIYUKI, ET AL., "A Quasi-Matrix Ferroelectric Memory for Future Silicon Storage," IEEE Journal of Solid-State Circuits, Vol. 37, No. 11, November 2002, pp. 1479-1484.	
	AM	PARK, KI-TAE, "Recent Non-Volatile Memory Device & Circuit Technology," Halo LSI Inc, (date unknown), 35 pages.	
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Examiner Initials*	Cite No. <sup>1</sup>	Include name of author (in CAPITAL LETTERS), title of article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
	AO	SHIN, JONGSHIN, ET AL., "A New Charge Pump Without Degradation in Threshold Voltage Due to Body Effect," IEEE Journal of Solid-State Circuits, Vol. 35, No. 8, August 2000, pp. 1227-1230.	
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